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# MS-7829

## Version : 1.1

### CPU :

**Intel Haswell Processor**

### System Chipset :

**Intel Lynx Point Chipset**

### On Board Chipset :


**VRM 12.5 --ISL95816HRZ 4 Phase**  
**Gigabit Intel Clarkville-V I217**  
**HDA Codec -- Realtek ALC662-VD**  
**Super I/O -- NCT5537D**  
**SPI Flash 64Mb**

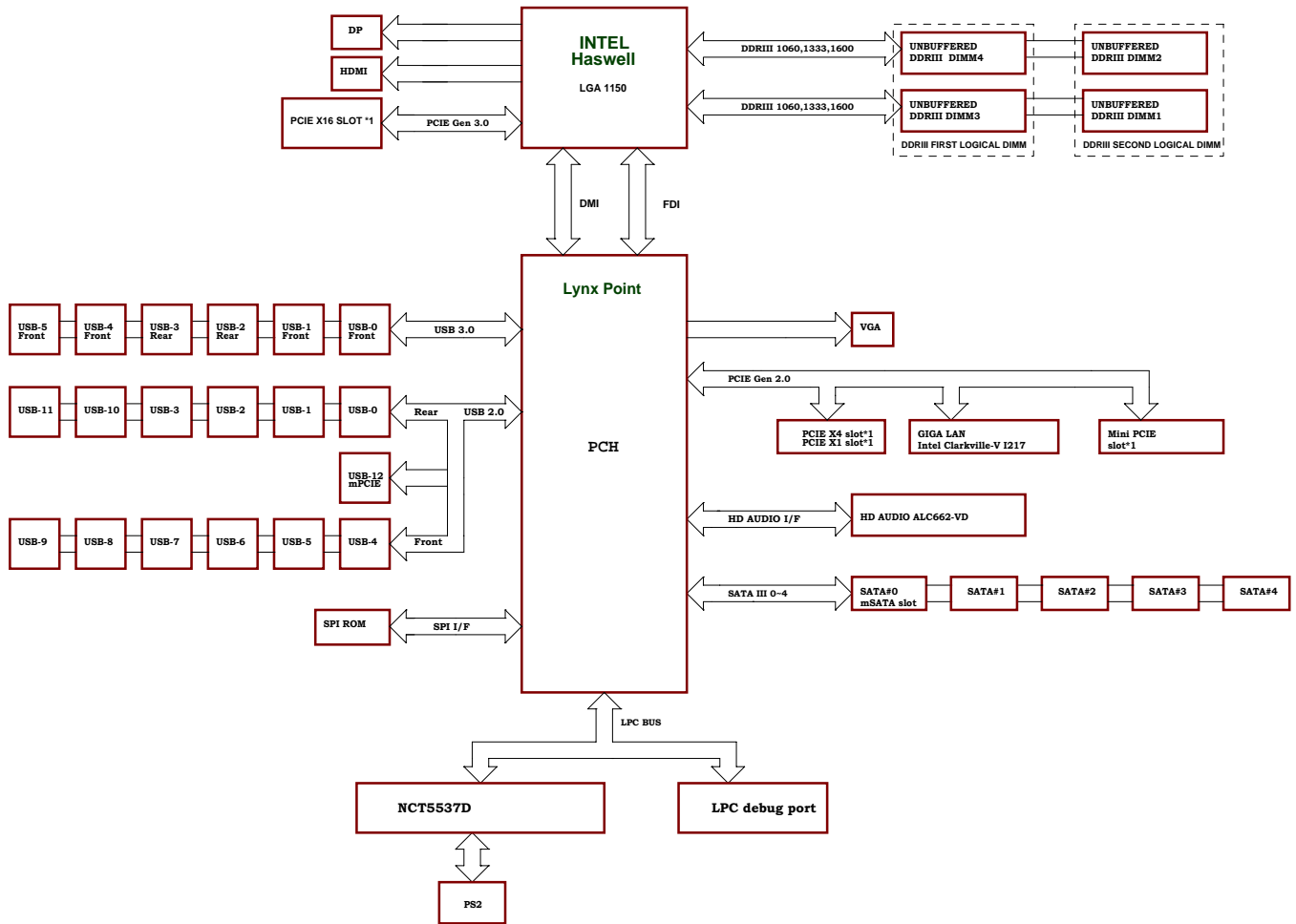
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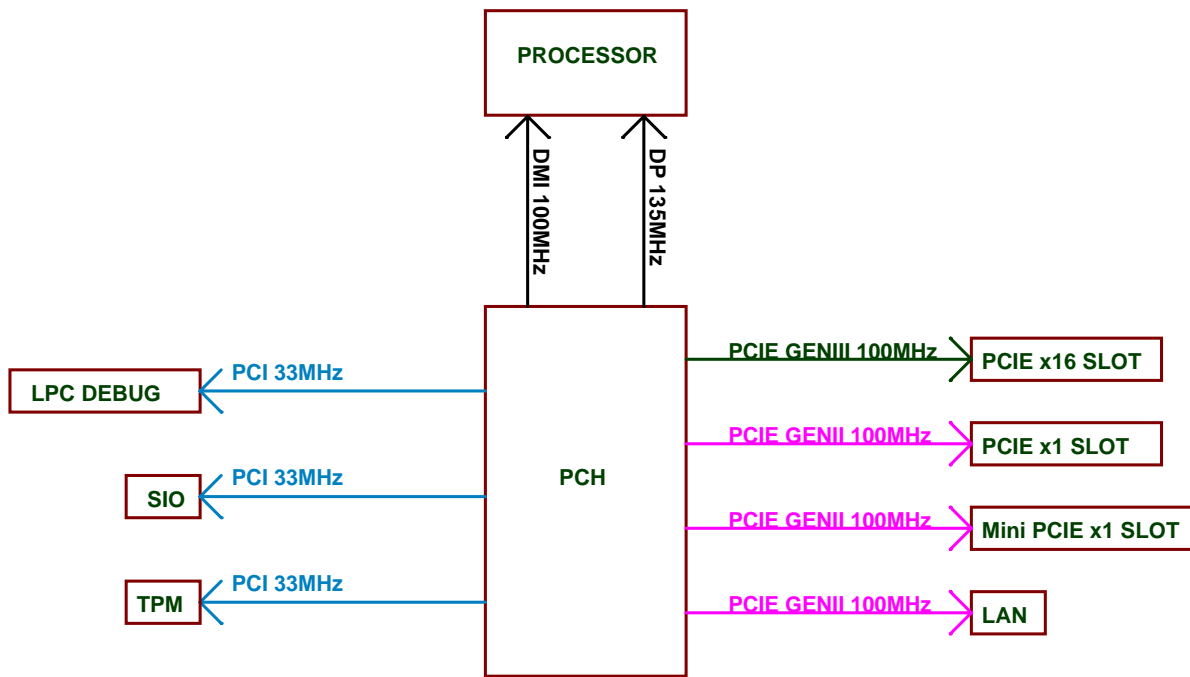
**2 Channel DDR III \* 4 (Max 16GB)**

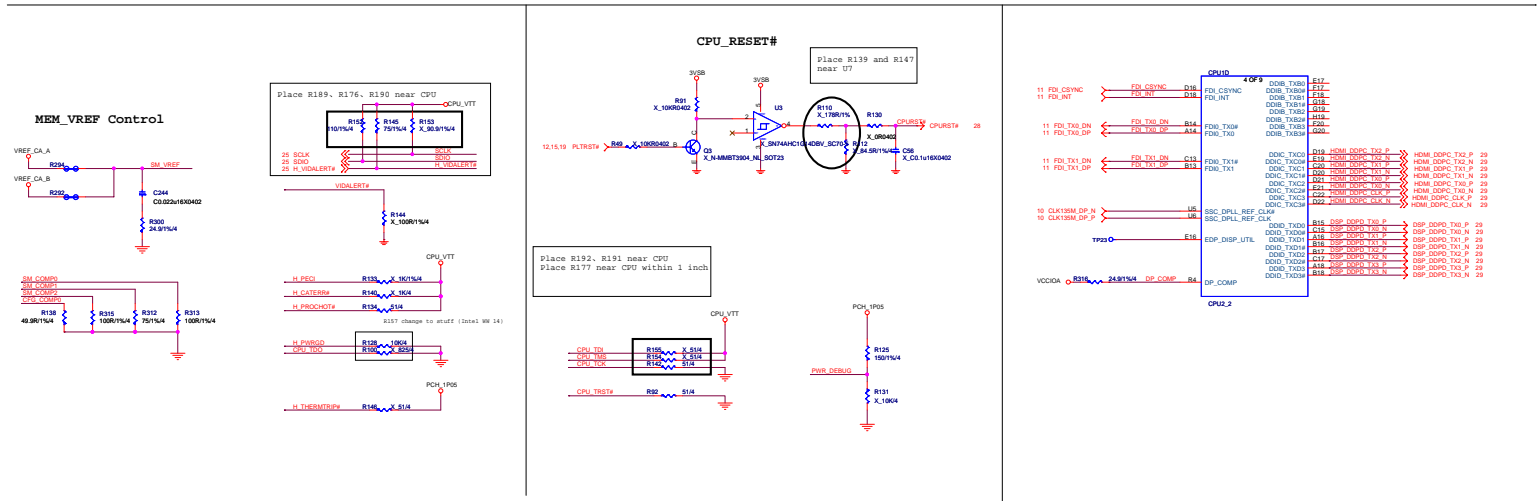
### Expansion Slot :

**PCI Express x16 Slot \* 1**  
**PCI Express x1 Slot \* 2**  
**Mini SATA Slot \* 1**  
**Mini PCIE Slot \* 1**

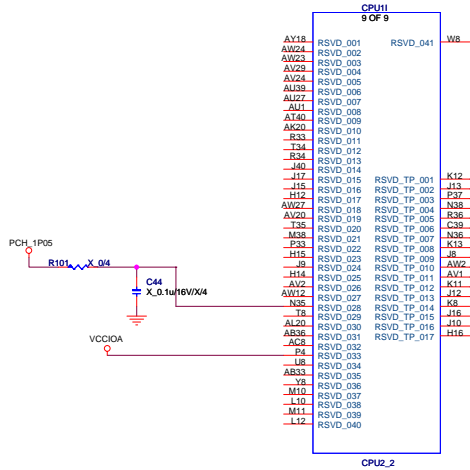
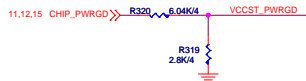
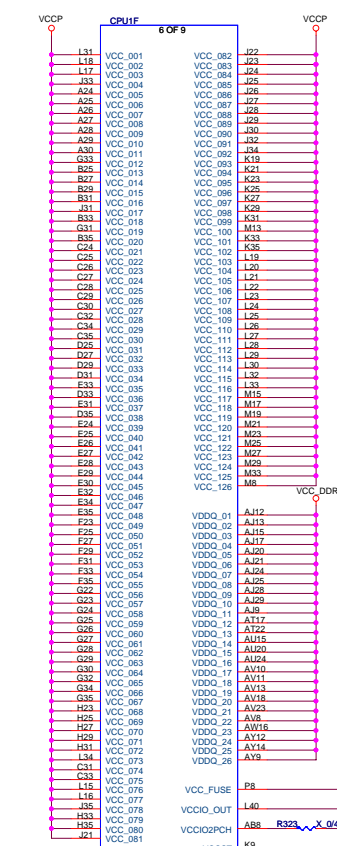
 <b>MICRO-START INTL CO.,LTD.</b>		
File <b>Cover Sheet</b>		
Size	Document Number	Rev
	<b>Acer SharkBay</b>	<b>1.1</b>
Date: Wednesday, December 19, 2012 Sheet 1 of 36		



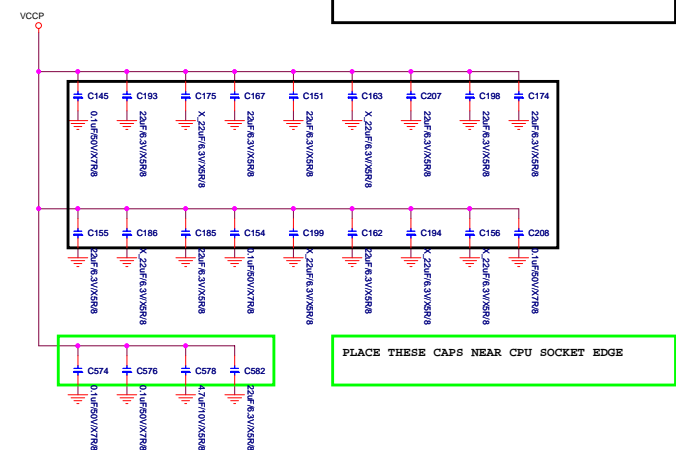




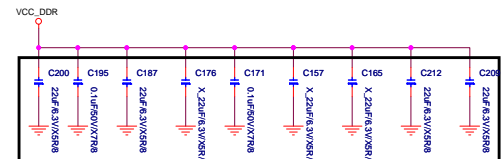


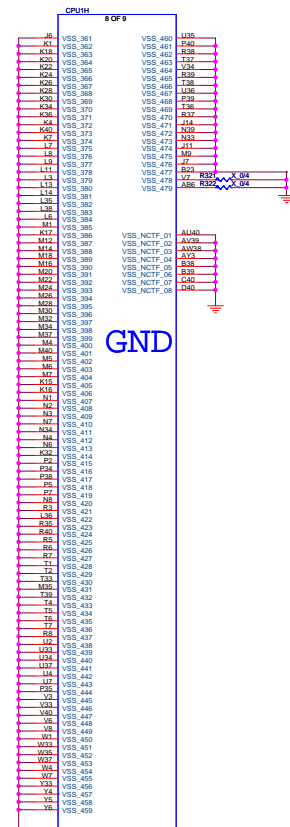
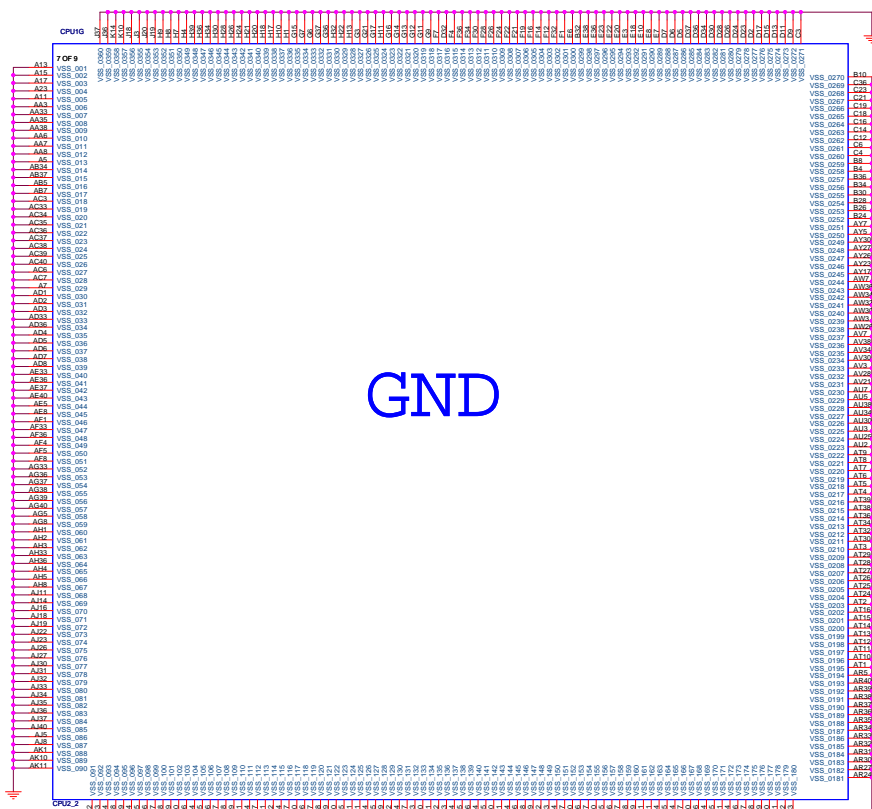


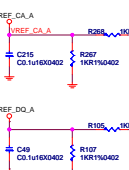
# VCCP-Decoupling



# VCC\_DDR-Decoupling

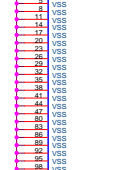







## DDR3 DIMM

The diagram shows a signal trace for VCC\_DDR, which is a constant high voltage level, represented by a solid blue line.

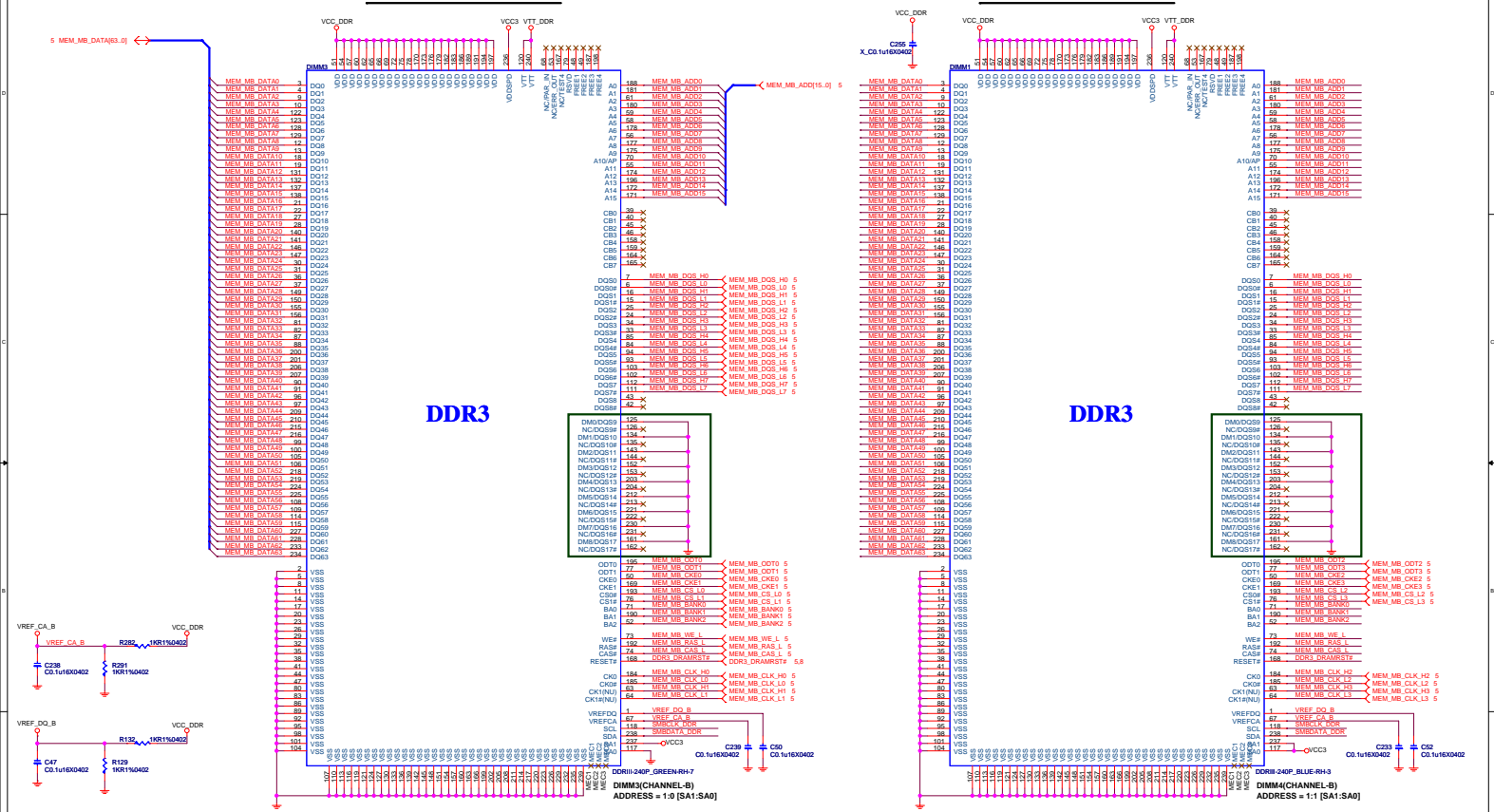


 <b>MSI</b> <i>Made in the Future</i>				<b>MICRO-START INTL CO.,LTD.</b>			
<b>Title</b> <b>DDR III DIMM 1 / DIMM 2</b>							
<b>Size</b>		<b>Document Number</b> <b>Acer SharkBay</b>				<b>Rev</b> <b>1.1</b>	
<b>Date</b>		<b>Wednesday, December 19, 2012</b>		<b>Sheet</b>		<b>8 of 35</b>	

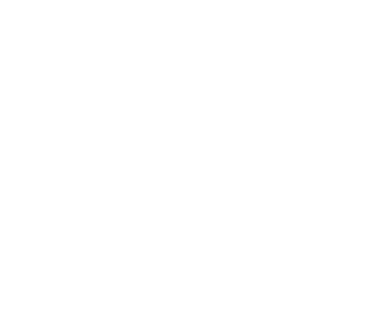
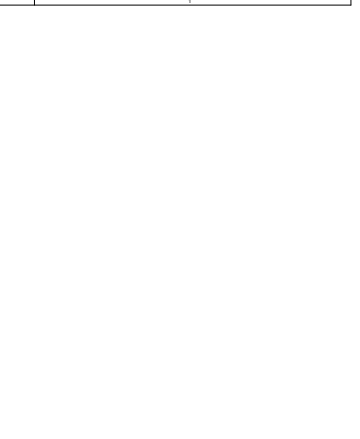
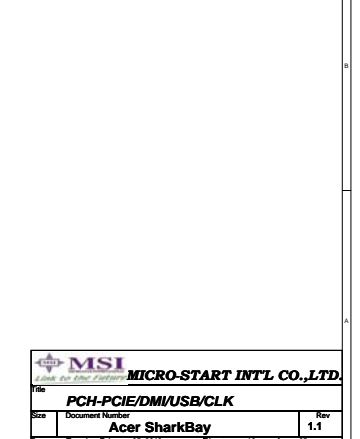
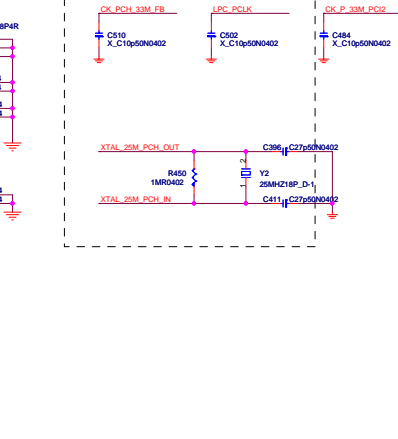
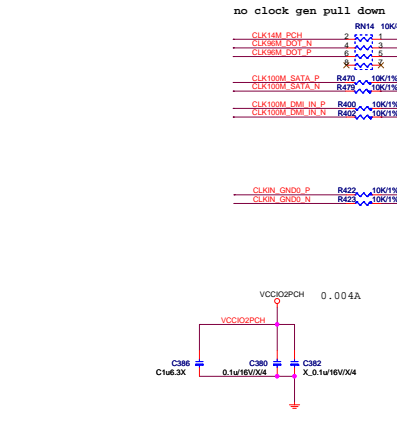
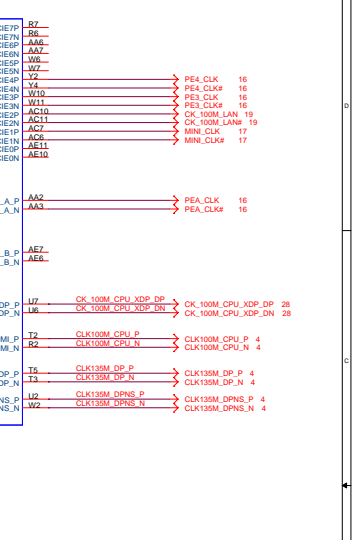
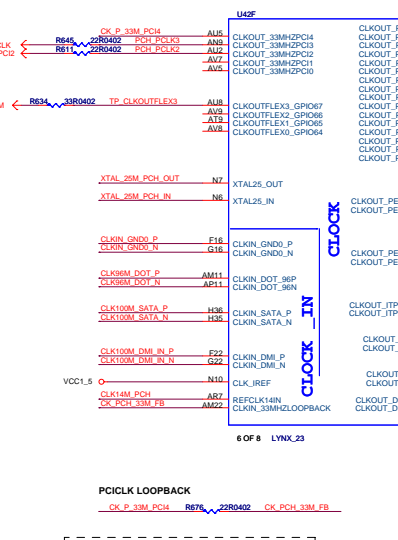
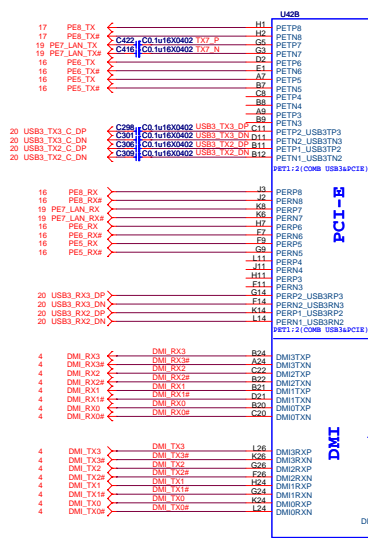


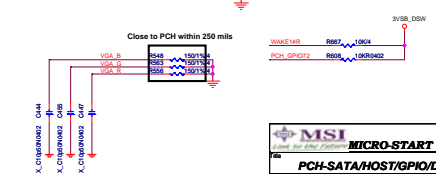
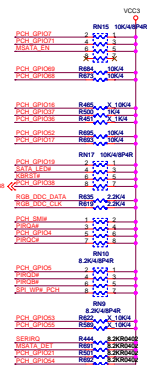
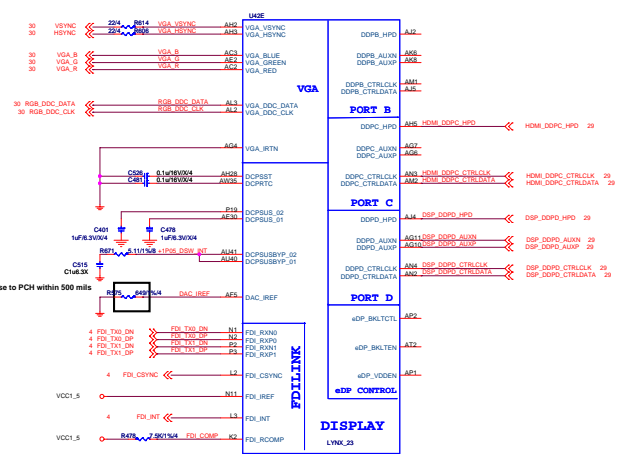
# DDR3 DIMM B1

# DDR3 DIMM B2

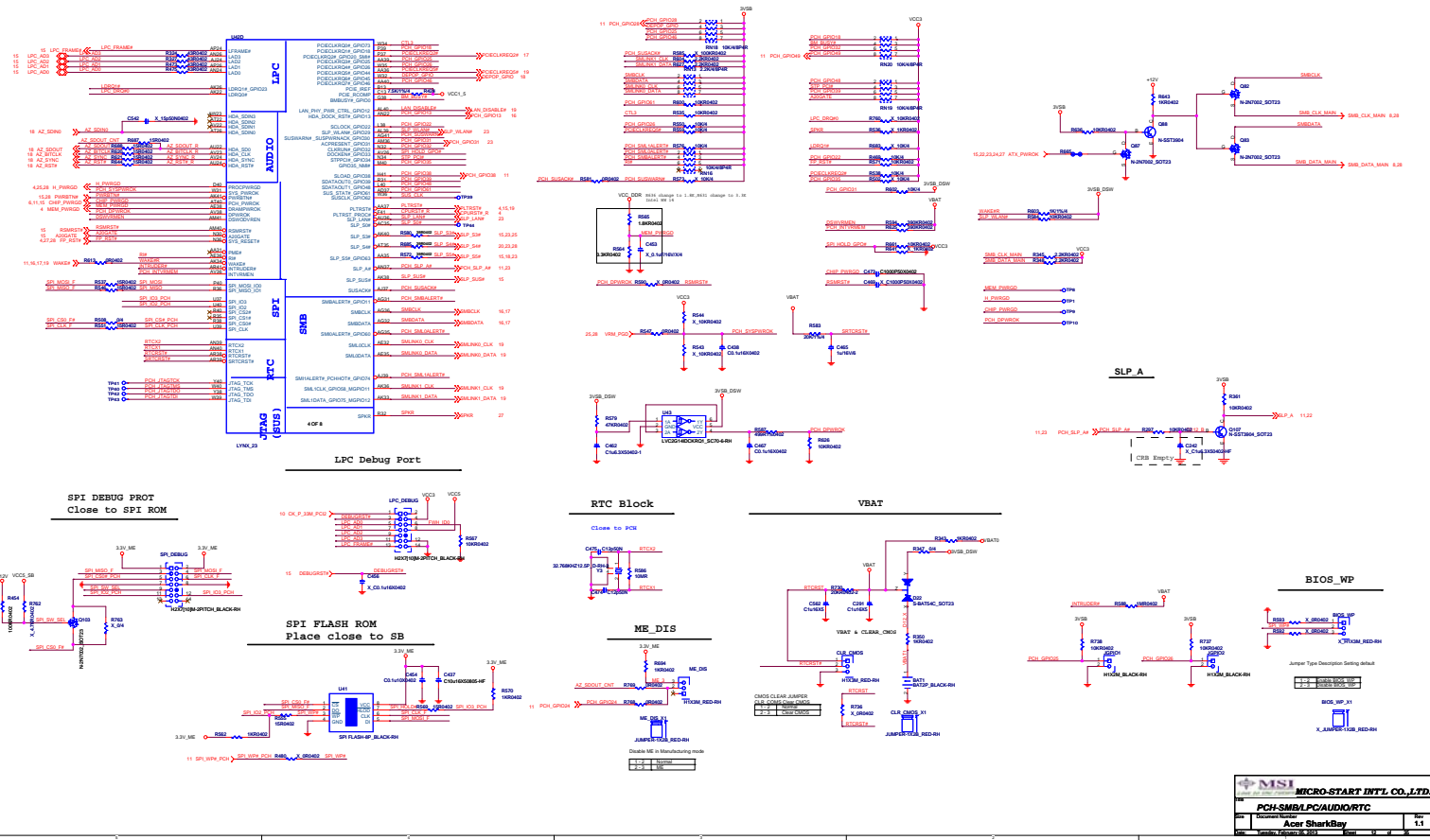


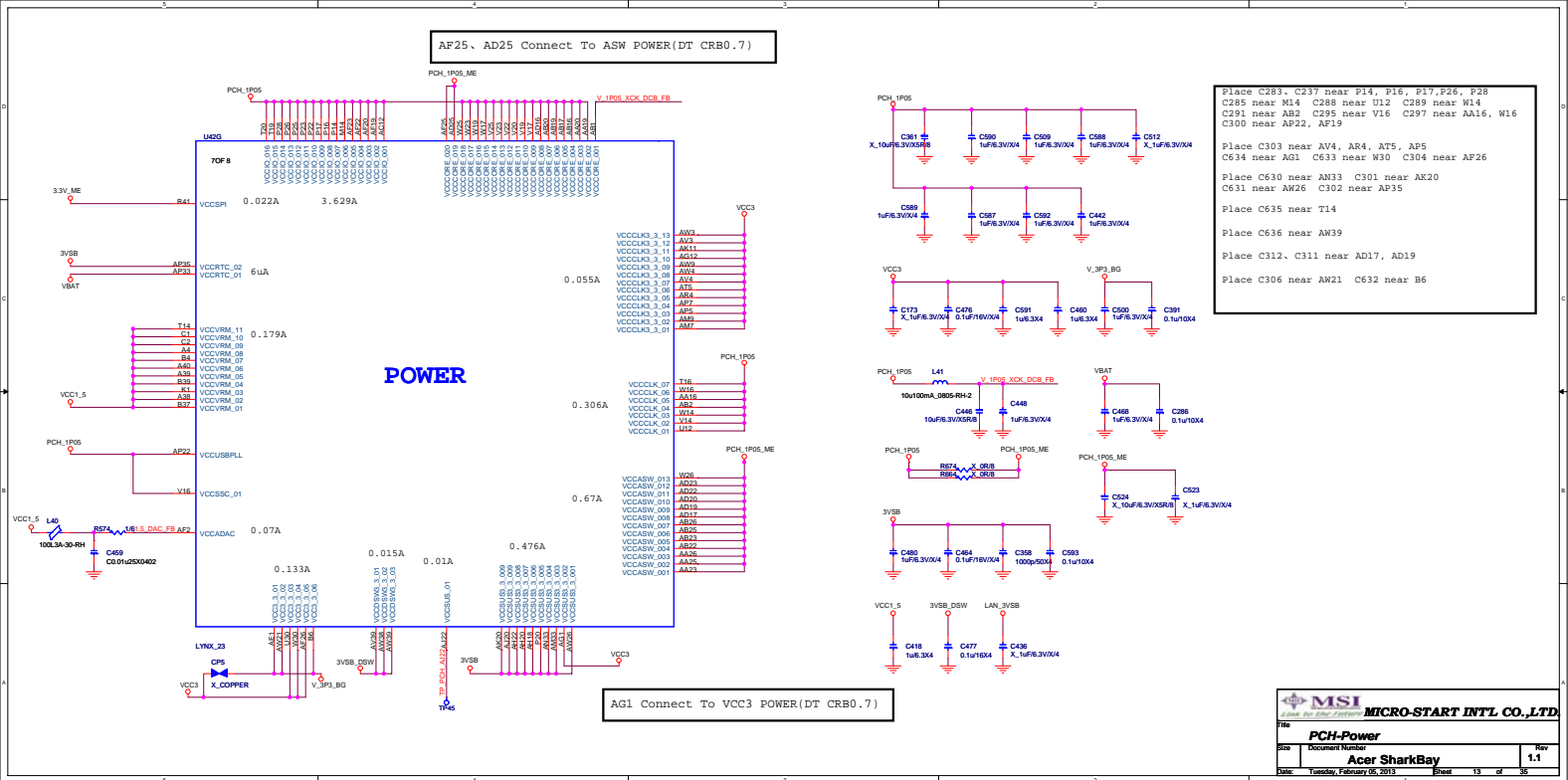
DDR3 DIMM B1  
DDR3 DIMM B2



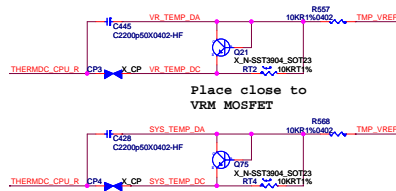
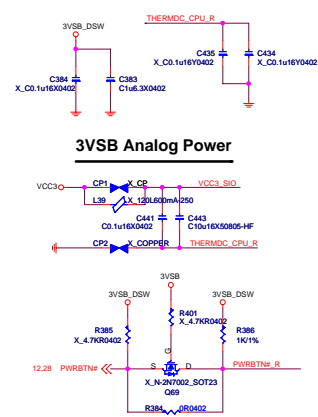
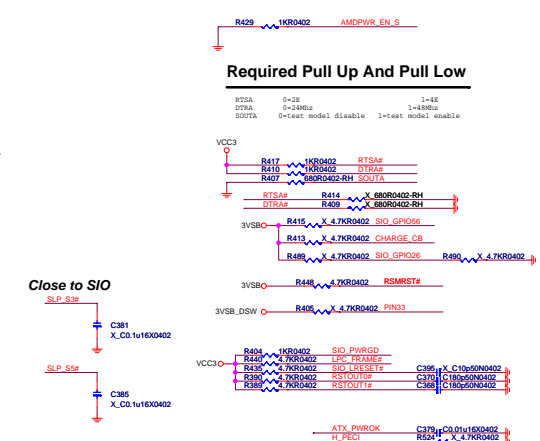
BIOS Device Select

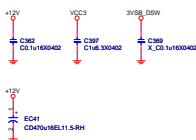
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1





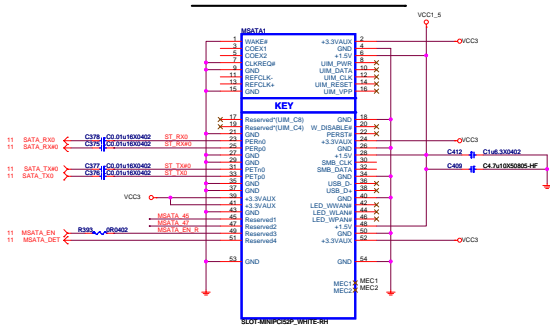




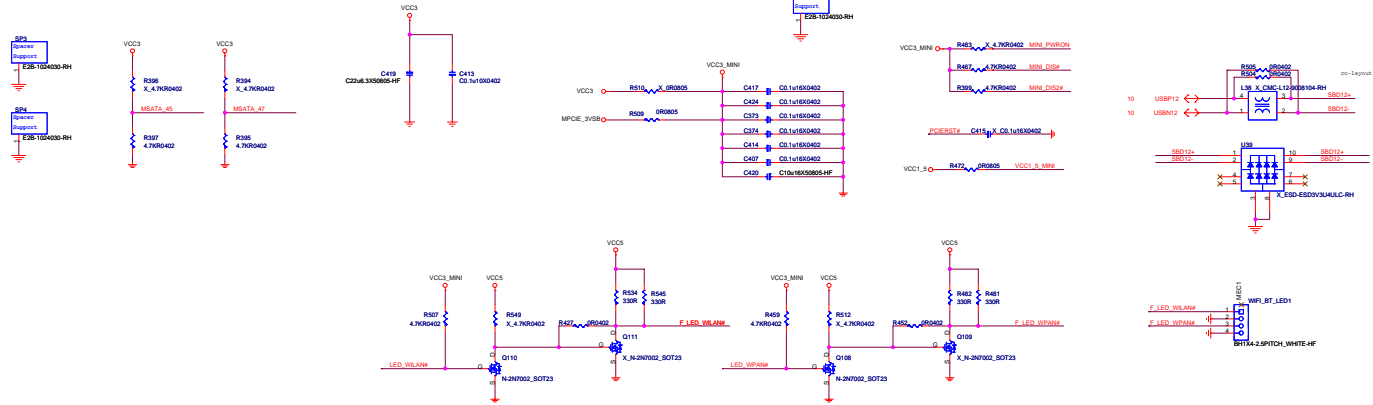
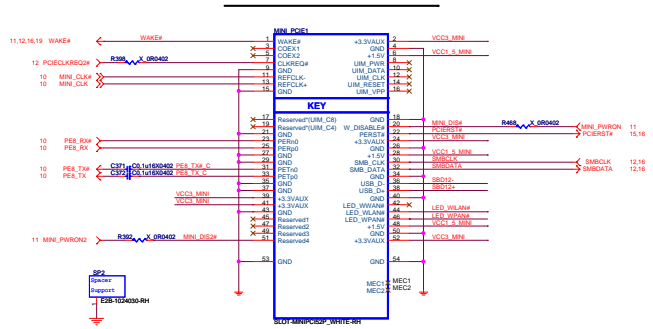
[illegible][illegible][illegible]



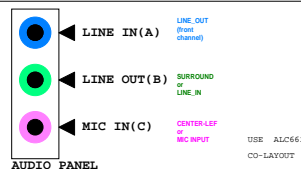
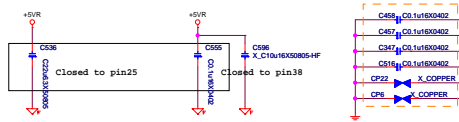
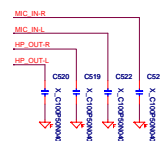
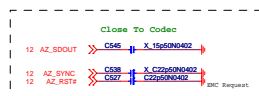
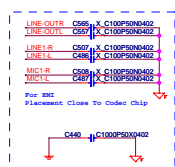
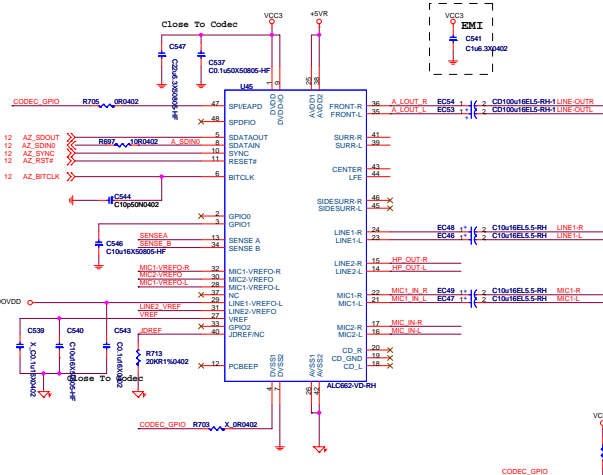
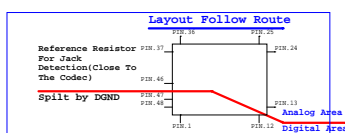
## Full-size Mini SATA Card



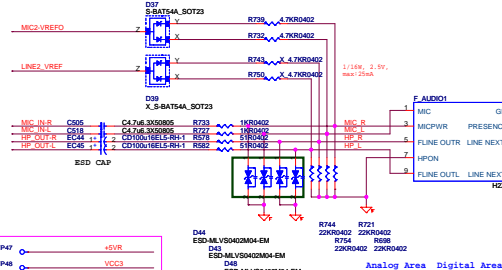
## Half-size Mini PCIe Card



## Azalia Codec -ALC662

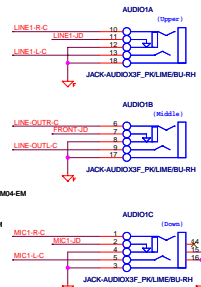


### Front Audio Jack

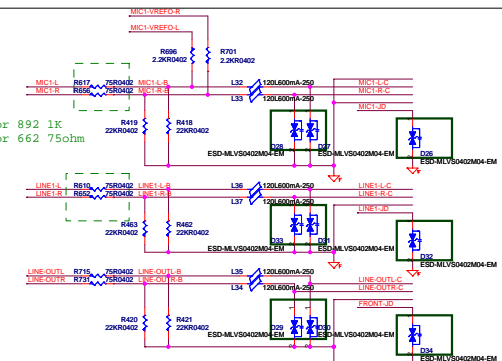
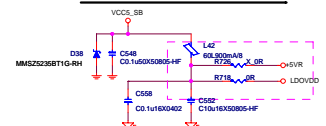


## EMC Request

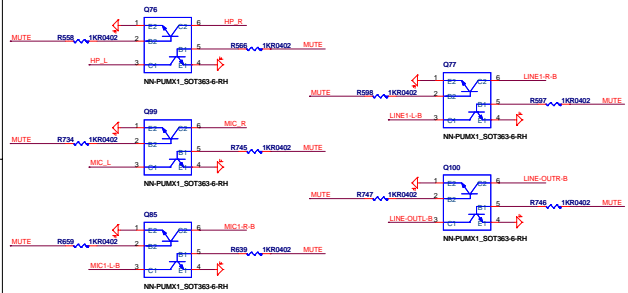
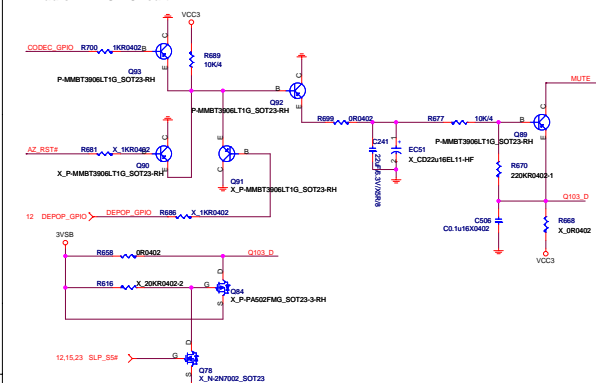
3 Jack Colay 6 Jack

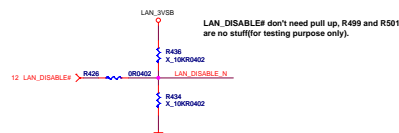


### AUDIO CODE REGULATORS

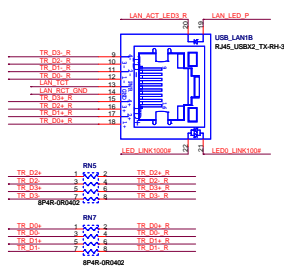


### Audio DE-POP Circuit

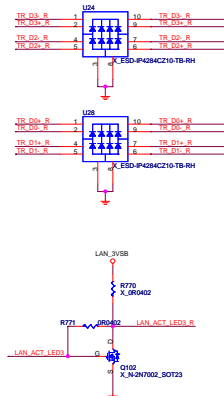




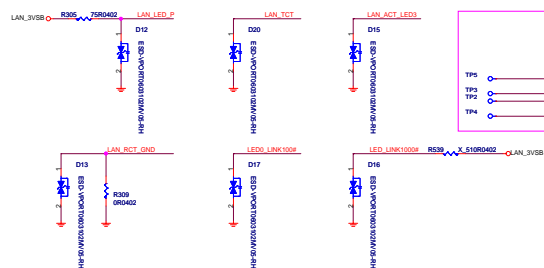
## LAN Connector



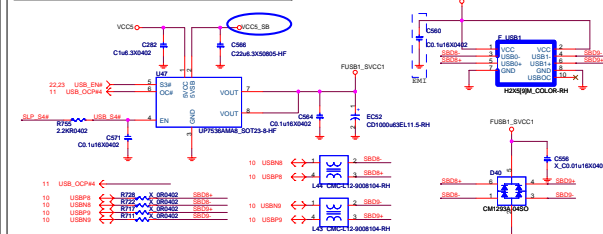
**ESD**



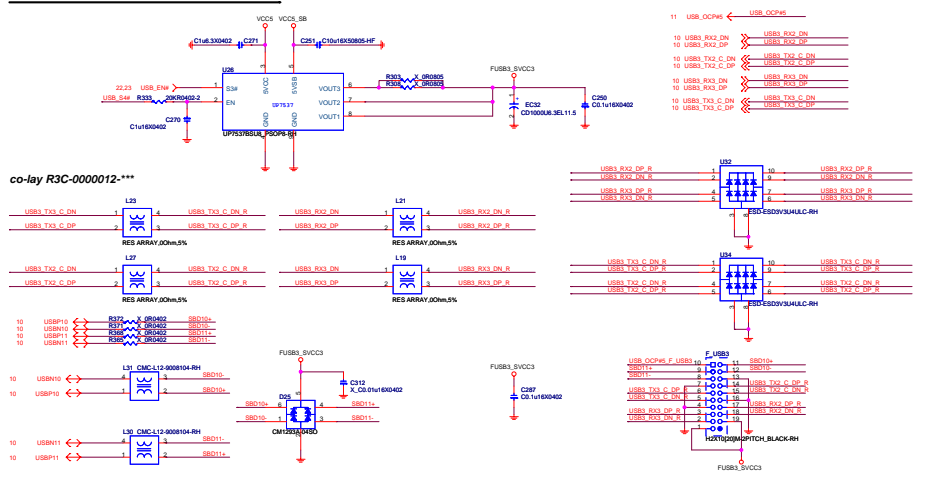
**ESD**



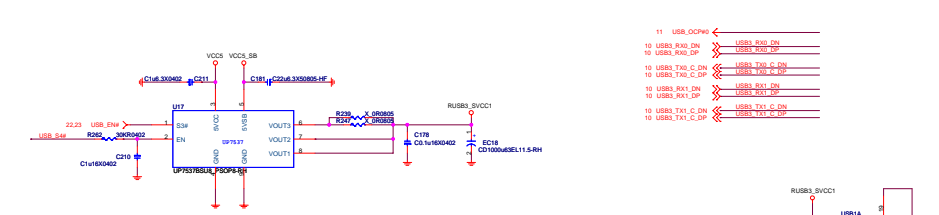
Front Panel USB Connector For USB Port 6 / 7



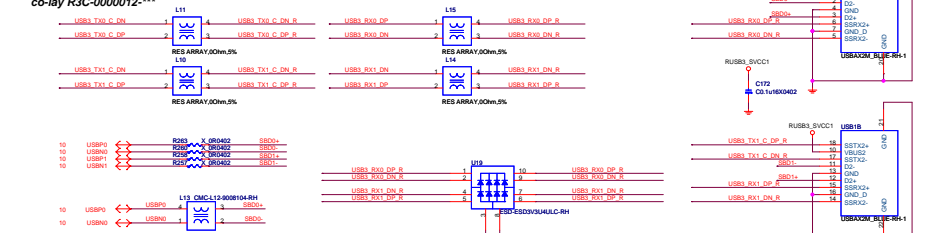
Front Panel USB Connector For USB Port 10 / 11



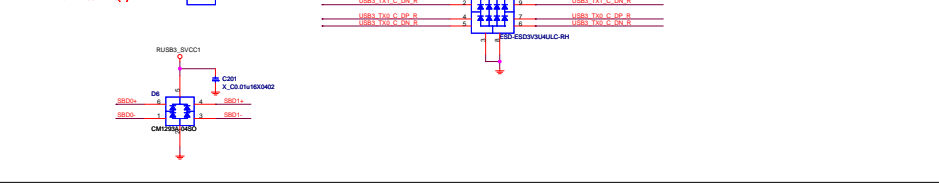
Rear USB Connector For USB Port 6 / 7



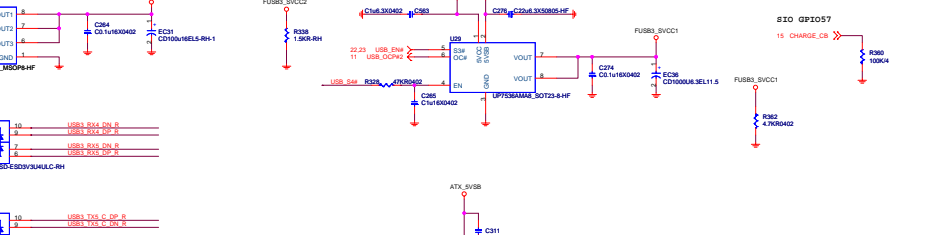
Rear USB Connector For USB Port 10 / 11



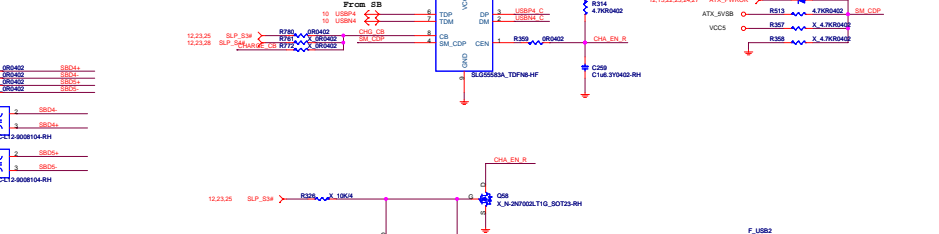
Rear USB Connector For USB Port 4 / 5



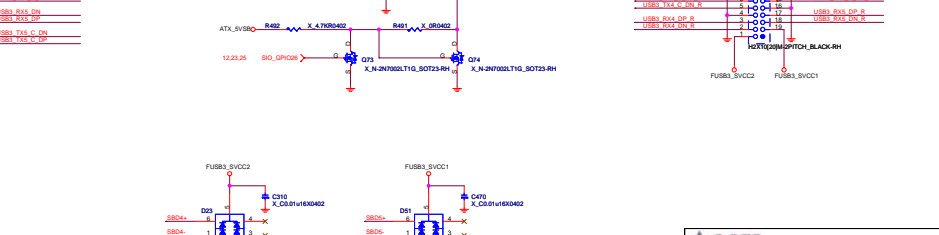
Rear USB Connector For USB Port 6 / 7



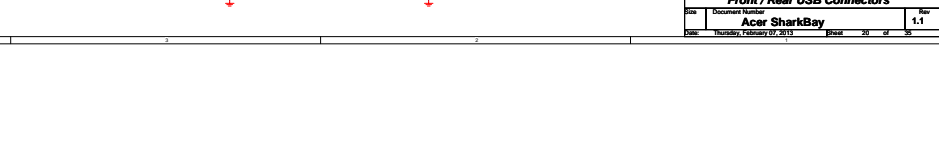
Rear USB Connector For USB Port 10 / 11



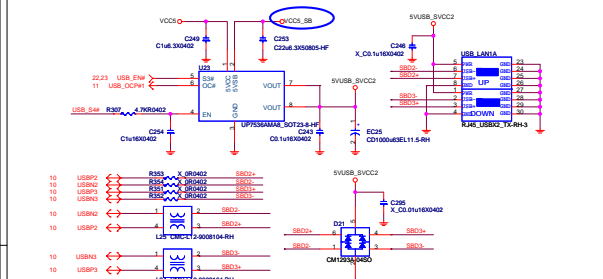
Rear USB Connector For USB Port 4 / 5



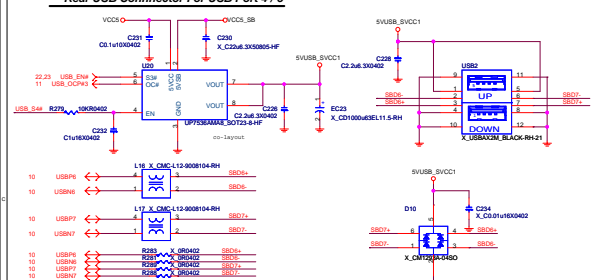
Rear USB Connector For USB Port 6 / 7



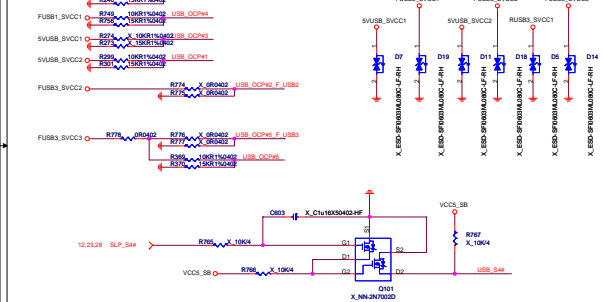
Rear USB Connector For USB Port 10 / 11



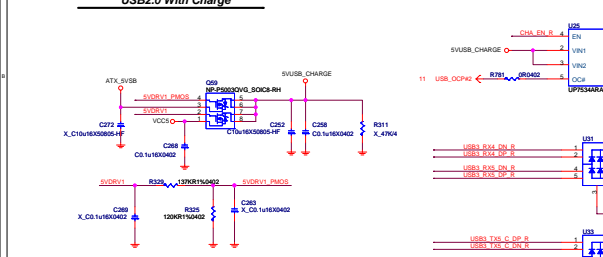
Rear USB Connector For USB Port 4 / 5



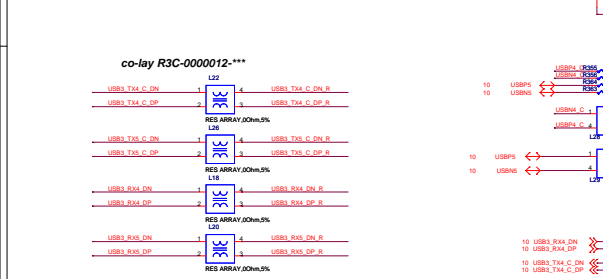
Rear USB Connector For USB Port 6 / 7



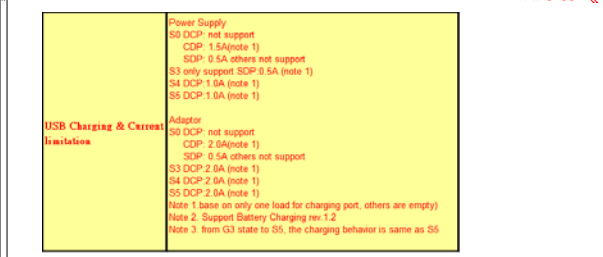
Rear USB Connector For USB Port 10 / 11



Rear USB Connector For USB Port 4 / 5



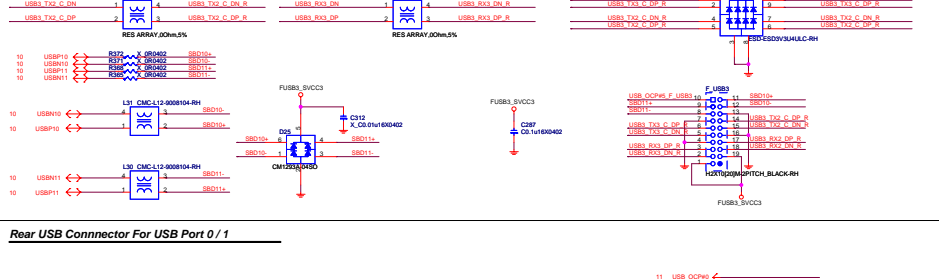
Rear USB Connector For USB Port 6 / 7



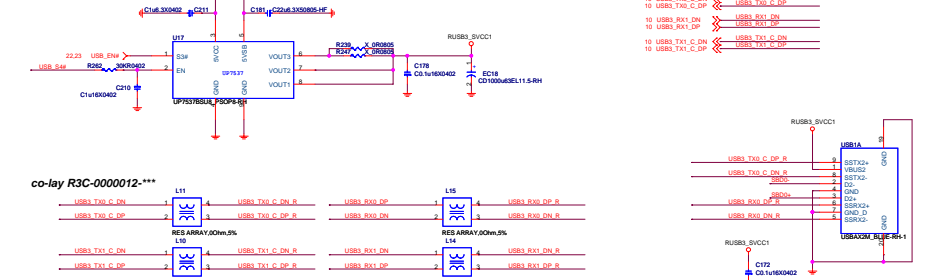
Rear USB Connector For USB Port 10 / 11



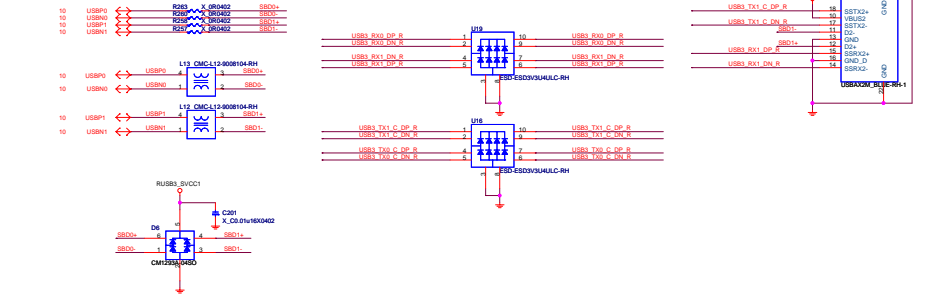
Rear USB Connector For USB Port 10 / 11



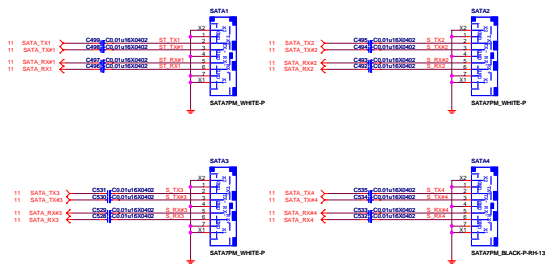
Rear USB Connector For USB Port 4 / 5



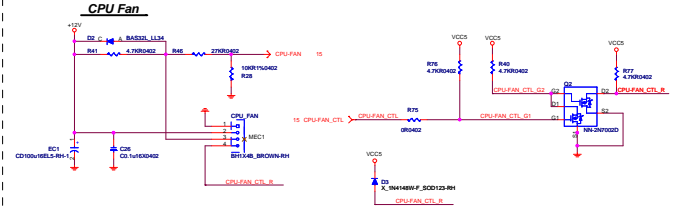
Rear USB Connector For USB Port 6 / 7



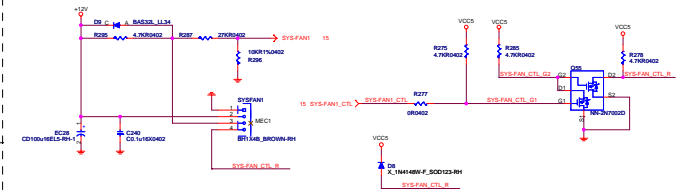
# SATA Connector



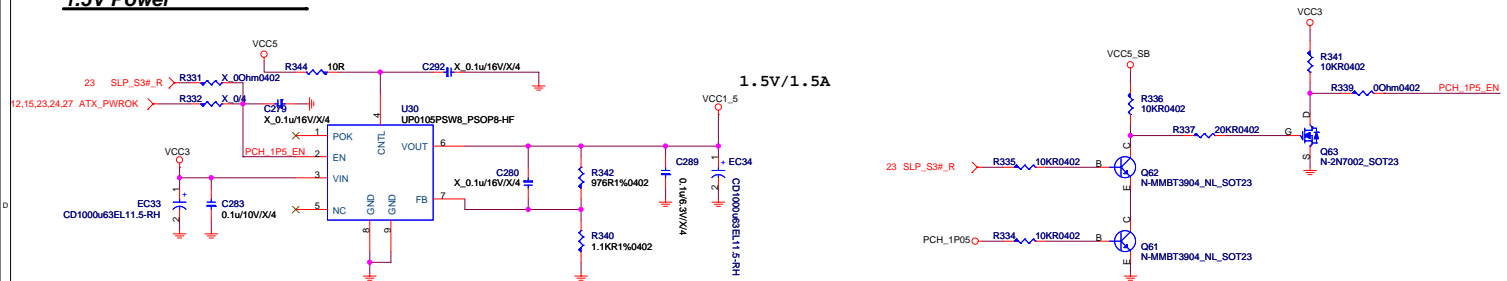
# CPU Fan



# System Fan

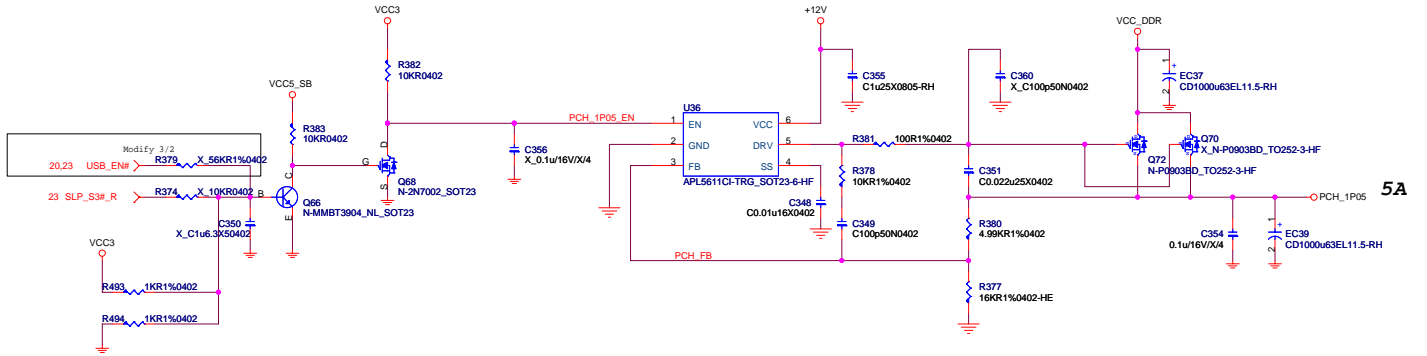


## 1.5V Power

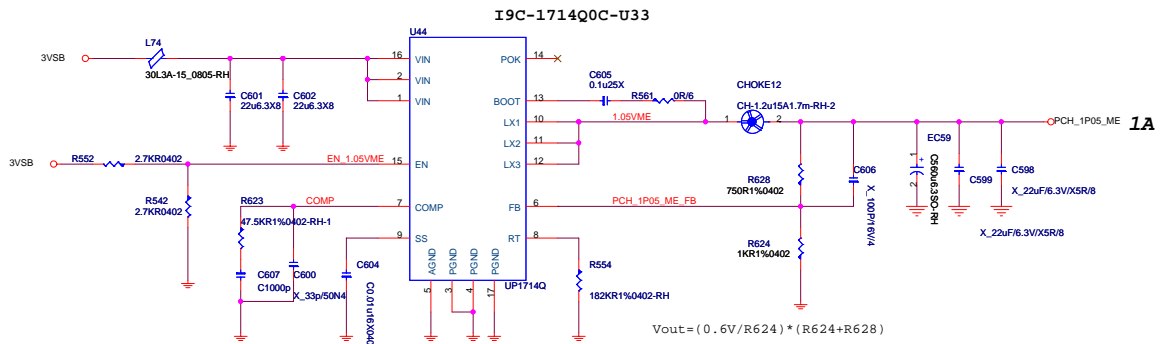


## PCH Core Power Control

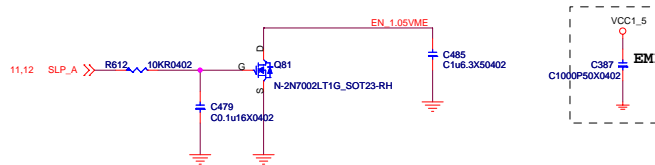
## PCH Core Power

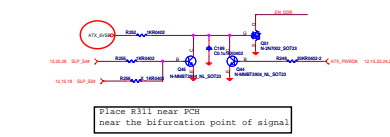
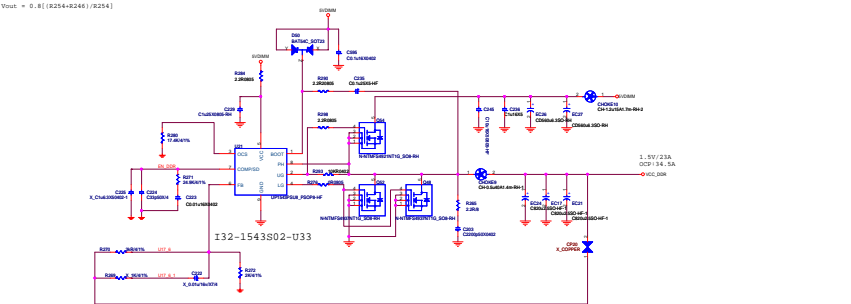


## PCH ME Power



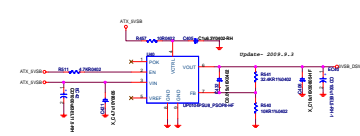
## PCH ME Power Control



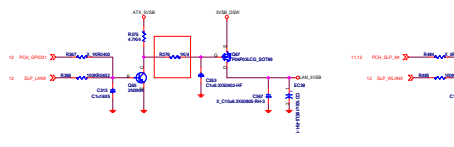


Deep Sx Power For Wake On Lan

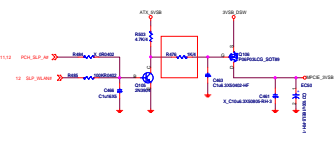
Vout=0.81 (0.461+0.449) / 0.461+0.392 V



LAN Power

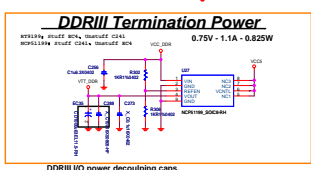
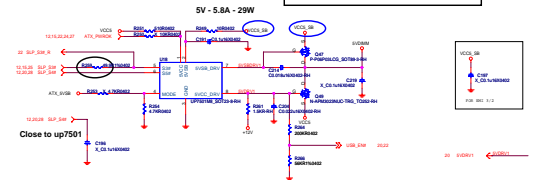


MPCIE Power

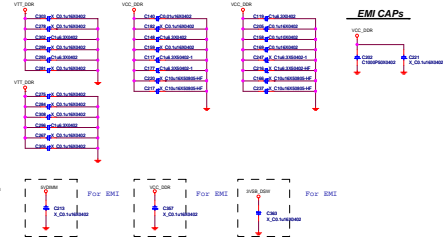


DDRIII Regulator Power Source

Place R86 near PCB, near the bifurcation point of signal



DDRIII I/O power decoupling caps.



EMI CAPS

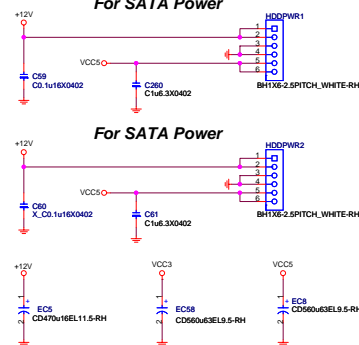




DCM programming pin:

- Ground this pin to setup automatic CCM-DCM transfer without minimum switching frequency limitation;
- Connect this pin to VCC to force CCM operation;
- Leave this pin open to give automatic CCM-DCM transfer, but with minimum switching frequency of 33KHz.

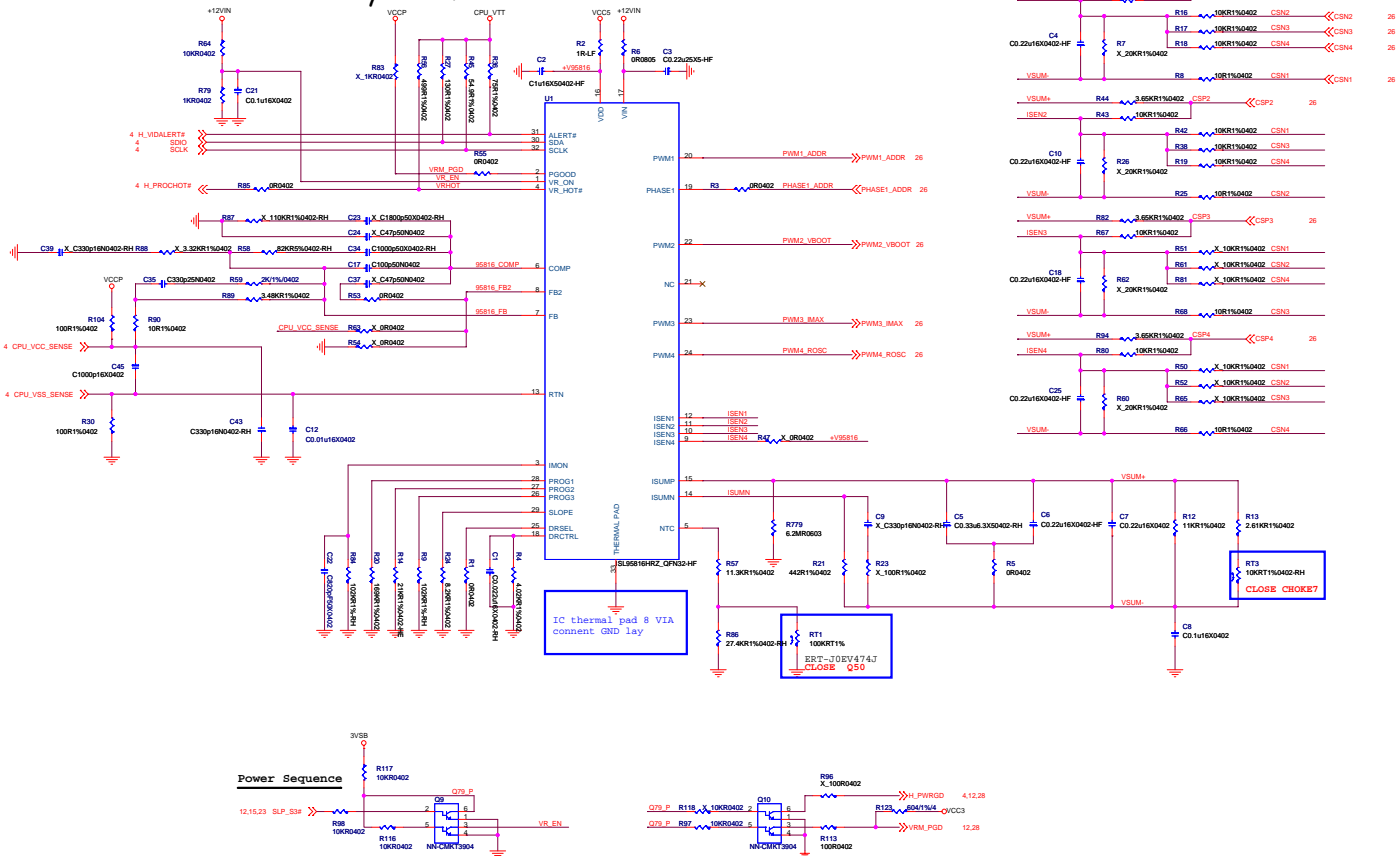
### VCC3&VCC5 Power Enable

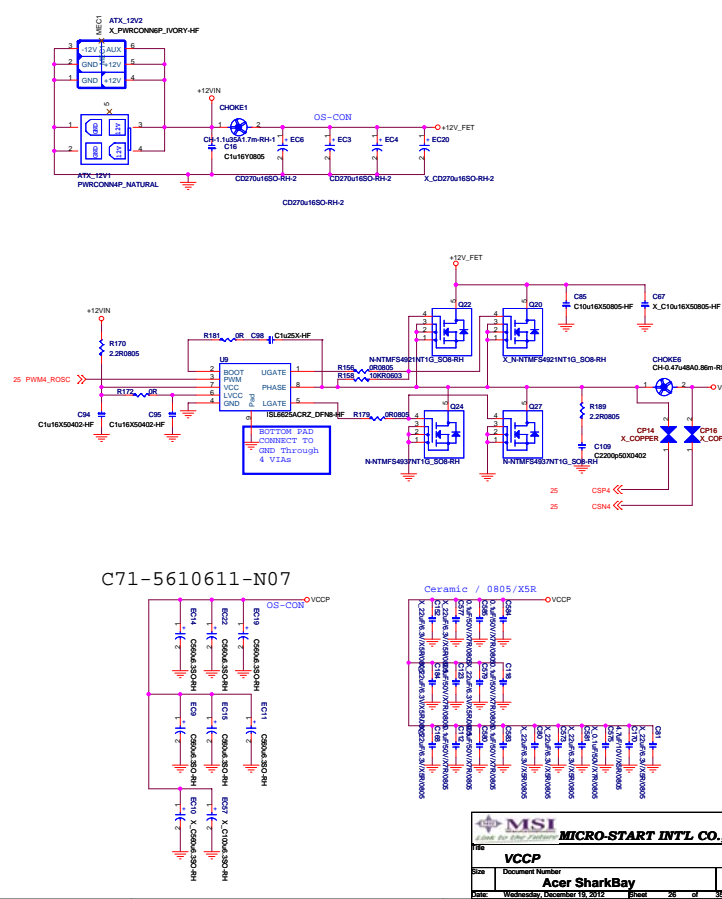


**For SATA Power**

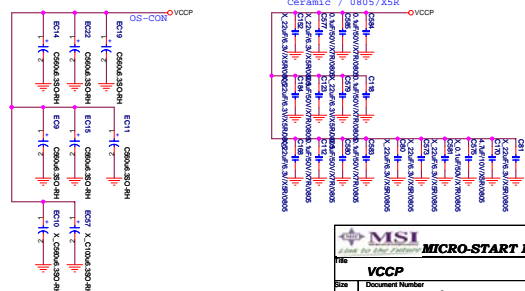


## SharkBay VR12.5 Power Circuit - 4 Phase



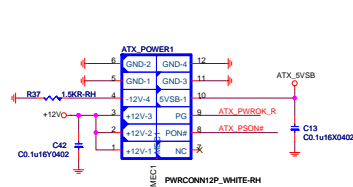


Ceramic / 0805/X5R



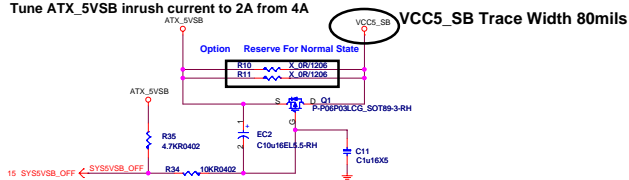
# ATX Power Connector / Front Panel / LED/DSW

## 12 Pin ATX Power Connector

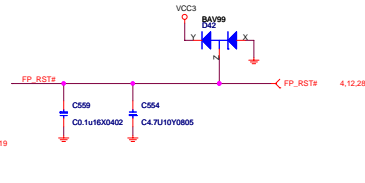
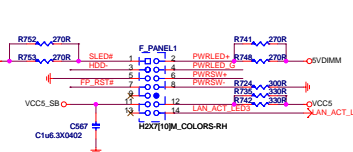


## 5VSB Power Switch

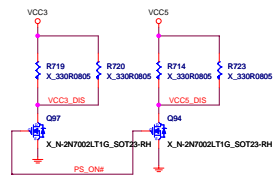
Tune ATX\_5VSB inrush current to 2A from 4A



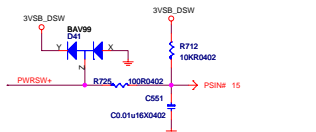
## Acer Front Panel Connector



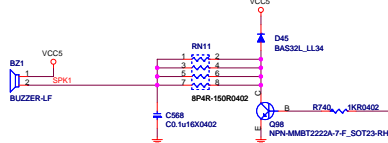
## VCC3, VCC5 Discharge Schematic



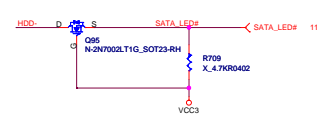
## Power Button



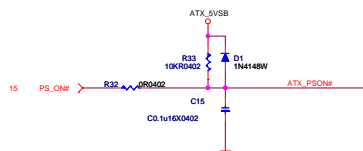
## Buzzer Circuit



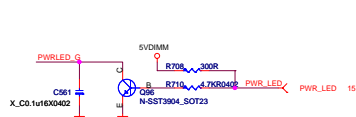
## HDD LED



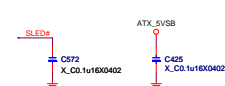
## ATX Power On

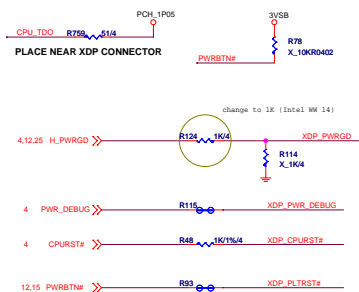
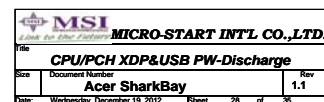


## Power LED

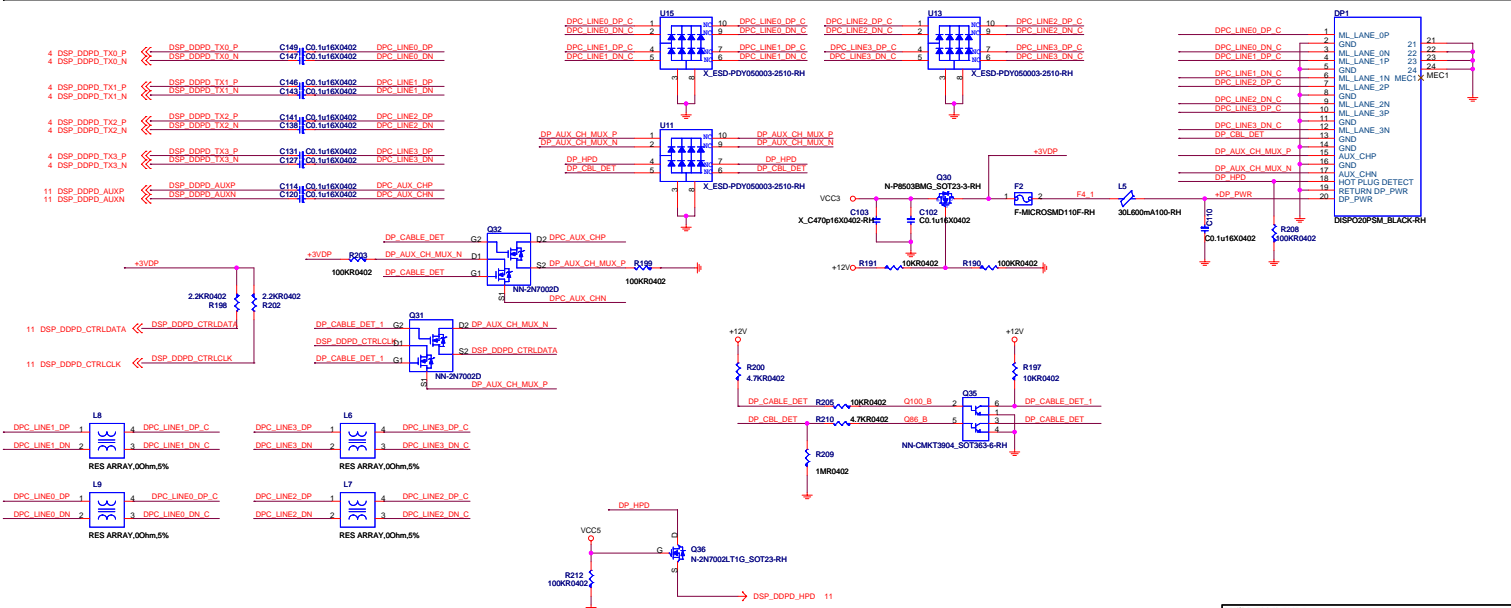
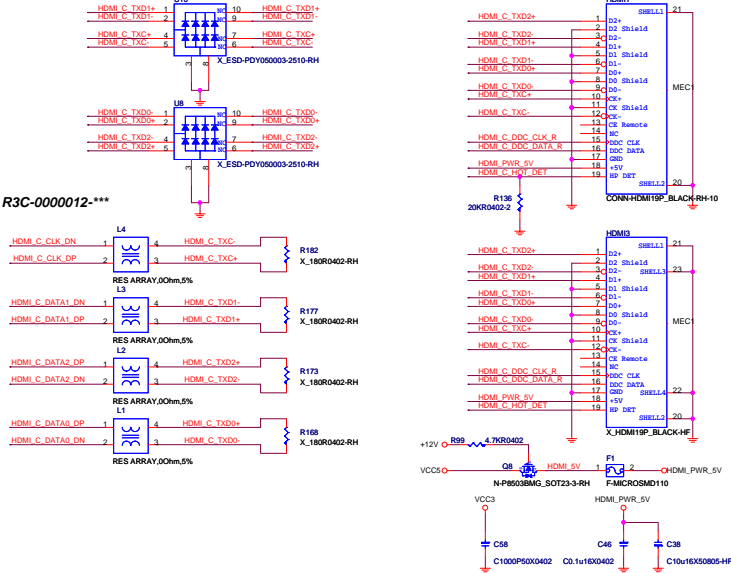
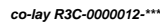
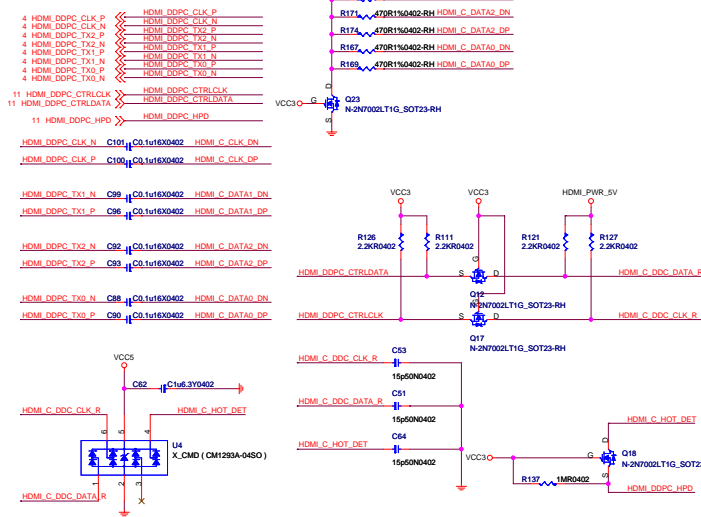


## Cap For EMI



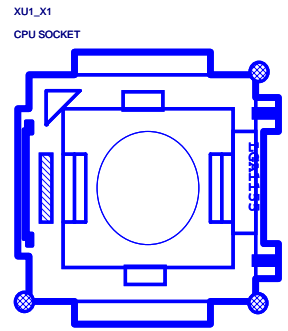
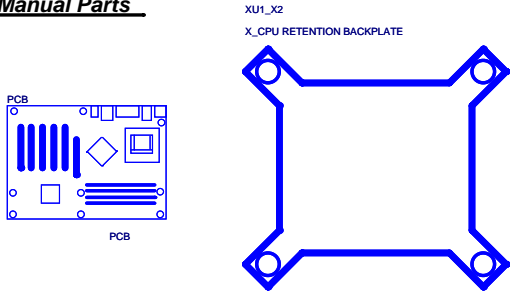
[illegible]

## HDMI level shifter





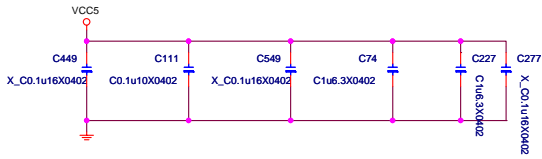
## Manual Parts



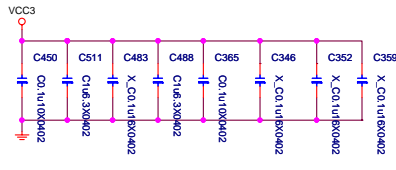
## Simulation



### For EMI

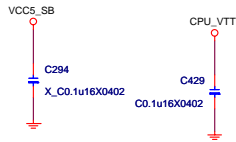


### For Moat CAP

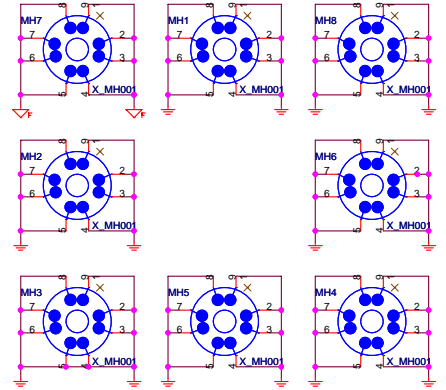


## Optics Orientation Holes

### Optical Fiducial Marks-120



## Mounting Holes



**MSI**  
Link to the Future

**MICRO-START INT'L CO.,LTD**

Title  
**Manual & Option Parts**

Size  
Document Number

Rev  
**1.1**

Date: Wednesday, December 19, 2012 Sheet 31 of 35

PCH						
GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BMBUSY#	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[1]	Unmuxed	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[2]	PIRQE#	I/O	Main	5V	GPI	SPL_WP#_PCH
GPIO[3]	PIRQF#	I/O	Main	5V	GPI	Pull-Hi
GPIO[4]	PIRQG#	I/O	Main	5V	GPI	Pull-Hi
GPIO[5]	PIRQH#	I/O	Main	5V	GPI	Pull-Hi
GPIO[6]	Unmuxed	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[7]	Unmuxed	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[8]	Unmuxed	I/O	Resume	3.3V	GPO	Pull-Hi
GPIO[9]	OC5#	I/O	Resume	3.3V	Native	USB_OCP#5
GPIO[10]	OC6#	I/O	Resume	3.3V	Native	USB_OCP#6
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	Native	LAN_DISABLE#
GPIO[13]	Unmuxed	I/O	Resume	3.3V	GPI	PCH_SMI#
GPIO[14]	OC7#	I/O	Resume	3.3V	Native	SIO_PME#
GPIO[15]	Unmuxed	I/O	Resume	3.3V	GPO	Pull-Hi
GPIO[16]	SATA4GP	I/O	Main	3.3V	GPI	Pull-Low
GPIO[17]	Unmuxed	I/O	Main	3.3V	GPI	CLR_CMOS
GPIO[18]	PCIECLKRQ1#	I/O	Main	3.3V	Native	Pull-Hi
GPIO[19]	SATA1GP	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[20]	PCIECLKRQ2#	I/O	Main	3.3V	Native	PCIECLKREQ2#
GPIO[21]	SATA0GP	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[22]	SCLOCK	I/O	Main	3.3V	GPI	LPT_DET#
GPIO[23]	LDRQ1#	I/O	Main	3.3V	Native	NC
GPIO[24]	Unmuxed	I/O	Resume	3.3V	GPO	MINI_PWRON
GPIO[25]	Unmuxed	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[26]	Unmuxed	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[27]	Unmuxed	I/O	DSW	3.3V	GPI	Pull-Hi
GPIO[28]	Unmuxed	I/O	Resume	3.3V	GPO	Pull-Hi
GPIO[29]	SLP_WLAN#	I/O	Resume	3.3V	Native	NC
GPIO[30]	SUS_PWRDN_ACK/SUS_WARN#	I/O	Resume	3.3V	GPI	PCH_SUSWARN#
GPIO[31]	Unmuxed	I/O	DSW	3.3V	GPI	Pull-Hi
GPIO[32]	Unmuxed	I/O	Main	3.3V	GPO	CLKRUN#
GPIO[33]	HDA_DOCK_EN#	I/O	Main	3.3V	GPO	Pull-Hi
GPIO[34]	STP_PCI	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[35]	Unmuxed	I/O	Main	3.3V	GPO	Pull-Hi
GPIO[36]	SATA2GP	I/O	Main	3.3V	GPI	NC

SIO(NCT5537D)

PIN NAME	USAGE	Input/Output	NOTES
GPIO0	AUX-FAN1_CTL	Output	Fan speed control
GPIO4	AUX-FAN1	Input	Fan speed sense
GPIO20	KBDATA	Input	Keyboard data in
GPIO21	KBCLK	Output	keyboard clock out
GPIO22	MSDATA	Input	Mouse data in
GPIO23	MSCLK	Output	Mouse clock out
GPIO24	SIO_WAKE#_R	Output	Wake up signal from LAN
GPIO25	AMDPWR_EN	Input	Pin strap which disabled AMD power sequence
GPIO26	SIO_GP26	Output	Reserved GPIO for future use
GPIO41	SMI#	Output	SIO SMI# generation
GPIO42	SDA_SIO	Output	Reserved GPIO for future use
GPIO54	SLP_SUS#	Input	DSW signal which received from PCH
GPIO56	PS2_DET#	Input	PS2 device detect signal
GPIO57	PWR_LED_R	Output	LED drive signal which shows the system state

SIO(NCT5537D)

PIN NAME	USAGE	Input/Output	NOTES
GPIO75	RSTOUT1#	Output	LPC_Debug card reset signal
GPIO76	RSTOUT2#	Output	TPM reset signal
GPIO80	CTSA#	Input	COM port signal
GPIO81	DSRA#	Input	COM port signal
GPIO82	RTSA#	Output	COM port signal
GPIO83	DTRA#	Output	COM port signal
GPIO84	SINA	Input	COM port signal
GPIO85	SOUTA	Output	COM port signal
GPIO86	DCDA#	Input	COM port signal
GPIO87	RIA#	Input	COM port signal

GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name
GPIO[37]	SATA3GP	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[38]	SLOAD	I/O	Main	3.3V	GPI	CHASSIS_ID1
GPIO[39]	SDATAOUT0	I/O	Main	3.3V	GPI	CHASSIS_ID2
GPIO[40]	OC1#	I/O	Resume	3.3V	Native	USB_OCP#1
GPIO[41]	OC2#	I/O	Resume	3.3V	Native	USB_OCP#2
GPIO[42]	OC3#	I/O	Resume	3.3V	Native	USB_OCP#3
GPIO[43]	OC4#	I/O	Resume	3.3V	Native	USB_OCP#4
GPIO[44]	PCIECLKRQ5#	I/O	Resume	3.3V	Native	PCIECLKREQ5#
GPIO[45]	PCIECLKRQ6#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[46]	PCIECLKRQ7#	I/O	Resume	3.3V	Native	ILIM_SEL
GPIO[48]	SDATAOUT1	I/O	Main	3.3V	GPI	COM_GPIO1
GPIO[49]	SATA5GP	I/O	Main	3.3V	GPI	MSATA_MPCIE_DET
GPIO[50]	Unmuxed	I/O	Main	3.3V	GPI	FUSB_G1
GPIO[51]	Unmuxed	I/O	Main	3.3V	GPO	NC
GPIO[52]	Unmuxed	I/O	Main	3.3V	GPI	FUSB_G2
GPIO[53]	Unmuxed	I/O	Main	3.3V	GPO	NC
GPIO[54]	Unmuxed	I/O	Main	3.3V	GPI	Pull-Hi
GPIO[55]	Unmuxed	I/O	Main	3.3V	GPO	NC
GPIO[57]	Unmuxed	I/O	Resume	3.3V	GPI	Pull-Hi
GPIO[58]	SML1CLK#	I/O	Resume	3.3V	Native	CTL1
GPIO[59]	SATA5GP	I/O	Resume	3.3V	Native	USB_OCP#0
GPIO[60]	SML0ALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[61]	SUS_STAT#	I/O	Resume	3.3V	Native	SUS_STAT#
GPIO[62]	SUSCLK	I/O	Resume	3.3V	Native	NC
GPIO[63]	SLP_S5#	I/O	Resume	3.3V	Native	SLP_S5#
GPIO[64]	CLKOUTFLEX0	I/O	CORE	3.3V	Native	NC
GPIO[65]	CLKOUTFLEX1	I/O	CORE	3.3V	Native	NC
GPIO[66]	CLKOUTFLEX2	I/O	CORE	3.3V	Native	NC
GPIO[67]	CLKOUTFLEX3	I/O	CORE	3.3V	Native	CLKOUTFLEX3_48M
GPIO[68]	Unmuxed	I/O	CORE	3.3V	GPI	Pull-Hi
GPIO[69]	Unmuxed	I/O	CORE	3.3V	GPI	Pull-Hi
GPIO[70]	Unmuxed	I/O	CORE	3.3V	GPI	MSATA_EN
GPIO[71]	Unmuxed	I/O	CORE	3.3V	GPI	Pull-Hi
GPIO[72]	Unmuxed	I/O	DSW	3.3V	Native	Pull-Hi
GPIO[73]	PCIECLKRQ0#	I/O	Resume	3.3V	Native	CTL3
GPIO[74]	SML1ALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[75]	SML1DATA	I/O	Resume	3.3V	Native	CTL2

DDR-III DIMM Config

DEVICE	ADDRESS(SA1:SA0)	CLOCK
DIMM 1	01	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 2	00	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 3	11	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 4	10	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1



Ver.OB history ( changed to OB from 0A)


1. Power solution  
<1>VRM  
R51 /R61 /R81 /R50 /R52 /R65 Change to NC  
R89 Change to 3.48K;R24 Change to 8.2K ;C7 Change to 0.22UF;R58 Change to 82k  
<2>DDR  
C234 Change to 470P;R271 Change to 2.43K,  
CH0KE9 Change to 0.5u/40A(P/N:L04-05A7211-L65)  
<3>SV  
R207 Change to 25.5K;R218 Change to 21K  
EC8/ EC13 Change to 560u(P/N:C71-5610611-N07)  
<4>JV  
R214 Change to 19.1K;R215 Change to 13K  
EC16 Change to 560u \*2 (Add 1pcs) P/N:C71-5610611-N07  
2. CPU Loading  
RT1 Change to 100K ohm(PW: R51-0104713-M05)  
R57 Change to 11.3k ohm(P/N: R11-1132712-W08)  
3. Add D50,For Memory power  
4. For card reader, (USB2.0 signal) USB 6 /7 and USB 10 /11 by Swap  
5. Audio  
<1>Stuff R698,R721  
<2>Reserve CS96  
<3>R617,R656 Change to 75 Ohm  
<4> Stuff R698; Reserve R668  
6. VCC\_DSB power change to up1534  
7. R169/R167/R174/R171/R175/R178/R180/R183 680 Ohm Change to 560 Ohm  
8. Reserve SLP\_S4# To U35.8  
9. Front USB3.0 header, RX-/RX- and TX-/TX- modify signal  
10. Front USB3.0 header,OP pin Change to Reserve  
11. USB power discharge circuit Change to Reserve  
12. MLC SIZE, C11-2267113-M09(5603) Change to C11-2267014-M09(0805)  
13. LAN Connector, pin21 and pin22 Swap  
14. R103 change to Reserve,For VCC3 Leakage voltage  
15. Add jumper setting, For BIOS\_WP  
16. LAN Power, PCH\_GPIO11 Stuff, SLP\_LAN# Reserve  
17. R446 and R447 Change to Reserve, Add R764(10K), For LAN\_3VSB Leakage voltage  
18. Reserve SLP\_S4# delay circuit, U26 and U29 EN pin use USB\_S4# control (page20)  
19. Stuff EC31  
20. ME Jumper, Reserve GPIO72 control  
21. Reserve LAN\_ACT\_LED1,L  
22. unmounts R413 , mount R360, For GPIO57 pull low  
23. CHARGE\_CB Add 0 ohm RESISTOR , R772  
24. R764 size 0402 Change to 0603, P/N: R11-0103033-W08.  
25. Front USB3.0 header,OP pin Change to Reserve  
26. R772 un-mount, R761 stuff

Ver.1.1 history ( changed to 1.1 from 1.0)

1. F\_USB2 protect diode modify Power separate,  
Picture 1(old V1.0 ) change to Picture 2(new V1.1)  
Picture 1(old V1.0 )  
Picture 2(new V1.1)  
2. ATX\_POWER1 change to P/N: N93-12M0091-H06. For the positioning column  
3. F\_USB3.0 header,P/N (Vendor P/N) : N32-2101091-H06 ( BH20NQ3BAFJ14 ) change to  
P/N (Vendor P/N) : N32-2101151-H06 (BH20NQ3GAPL14 )  
4. Modify BOM, Remove BIOS write protect and CIR header  
5. Modify BOM, Add Rear DP port

Ver.1.0 history ( changed to 1.0 from 0B)

1. LPC bus, PCH side False resistance change to 43 ohm ;  
SIO side False resistance change to 0 ohm  
2. SPI\_DEBUG change to P/N: N31-2071101-H06  
3. System fan 3pin change to 4pin  
3. VOA port NS1-15P0871-K06 Factories have reported : processing length pin problems exist; V1.0 change to  
P/N: NS1-15P0801-K06  
4. Switch power high/Low side Footprint change to SOT669\_COLAY  
5. USB3.0 BOX HEADER modify  
N31-2101211-H06 change to N32-2101091-H06  
6. For Acer IOAC function modify  
7. BIOS ROM  
R85 BOM:16M size; P/N: M31-2512853-W03  
Z87 BOM:8M size; P/N: M31-25Q6433-M03  
8. SATA#  
R85 BOM:BLACK; P/N: NSN-07M2081-L06  
Z87 BOM: WHITE; NSN-07M1881-L06  
9. ME\_DIS , change Reserve PCH\_GPIO24  
10. Power solution  
CORE  
R84=115K  
U1/ ISL95816, Pin15 (ISUMP Pin) Add 4.7M ohm to GND  
DDR  
R280=17.4K  
R271=24.9K  
(OCP=35.7A)  
VCC3  
R215=10K  
R214=11.6K  
(OCP=25.44A)  
VCC5  
R218=15K  
R207=16K  
(OCP=41A)  
11. SIO NCT5533D/NCT5537D Cancel Co-lay; stuff NCT5537D  
12. In deep S5 support USB charge, power modify to ATX\_5VSB  
Modify charge spec S3 state support DCP mode  
13. USB\_OCP#2 modify



**MICRO-START INTL CO.,LTD.**

Title

**History**

Size

Document Number

Rev

**Acer SharkBay**

**1.1**

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Thursday, December 20, 2012

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